Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Original) An asymmetric SRAM cell for storing a binary variable, the asymmetric SRAM cell having reduced leakage power with respect to a comparable symmetric SRAM cell when the asymmetric SRAM cell stores a binary variable representing a predetermined binary value, the asymmetric SRAM cell comprising:

a plurality of transistors operably coupled and configured as an asymmetric SRAM cell, wherein the plurality of transistors include at least one first type of transistor and at least one second type of transistor that is weaker than the first type of transistor, such that the configuration of the asymmetric SRAM cell achieves reduced leakage power with respect to a symmetric SRAM cell having the first type of transistor only.

2. (Original) The asymmetric SRAM cell of claim 1 wherein at least one of the second type of transistor is selected from among the group consisting of:

a transistor having a higher voltage threshold (V_t) as compared to the voltage threshold (V_t) of the first type of transistor;

a transistor having a decreased channel width as compared to the channel width of the first type of transistor; and

a transistor having an increased channel length as compared to the channel length of the first type of transistor.

3. (Original) A sense amplifier for coupling with an asymmetric SRAM cell that provides faster access times when the asymmetric SRAM cell stores a first predetermined binary value, said sense amplifier comprised of:

a first pair of cross coupled inverters across a bitline (BL) and a bitline bar (BLB);

a second pair of cross coupled inverters operably coupled with the first pair of cross coupled inverters;

a plurality of additional transistors forming a dummy column of cells that store a second predetermined binary value at all times wherein during a read operation of the SRAM cell one of

the dummy cells will have its wordline asserted, said dummy column of cells operably coupled with the first pair of cross coupled inverters; and

four inputs operably coupled with a subset of transistors of the sense amplifier wherein the inputs include the BL, the BLB that derive from the SRAM cell, a dummy bit line (D), and a dummy bitline bar (DB) that are input to the dummy cells such that D is input to the sense amplifier on the same side as BLB while DB is input to the sense amplifier on the same side as BL.

4. (Original) The sense amplifier of claim 3 wherein at least one of the transistors coupled with BL and BLB have higher transconductance characteristics than at least one of the transistors coupled with D and DB.

5. (Original) The sense amplifier of claim 3 wherein at least one of the transistors coupled with BL and BLB are selected from among the group consisting of:

transistors having a lower voltage threshold (V_t) as compared to the voltage threshold (V_t) of the transistors coupled with D and DB;

transistors having a increased channel width as compared to the channel width of the transistors coupled with D and DB; and

transistors having a decreased channel length as compared to the channel length of the transistors coupled with D and DB.

6. (Original) An SRAM device comprising:

an array of SRAM cells wherein each SRAM cell stores a binary variable representing a predetermined binary value, and each SRAM cell is an asymmetric SRAM cell having reduced leakage power with respect to a comparable symmetric SRAM cell, each asymmetric SRAM cell comprising:

a plurality of transistors operably coupled and configured as an asymmetric SRAM cell, wherein the plurality of transistors include at least one of a first type of transistor and at least one of a second type of transistor that is weaker than the first type of transistor, such that the configuration of each asymmetric SRAM cell achieves reduced leakage power with respect to a symmetric SRAM cell having the first type of transistor only.

7. (Original) The SRAM device of claim 6 wherein the array of SRAM cells in the SRAM device comprises an SRAM device selected from the group consisting of a direct store SRAM device and a selectively inverted SRAM device.

8. (Original) The SRAM device of claim 6 wherein the array of SRAM cells in the SRAM device comprises a cache memory selected from the group consisting of a direct store cache memory and a selectively inverted cache memory.

9. (Original) A combination SRAM device and sense amplifier comprising:

an array of SRAM cells wherein each SRAM cell stores a binary variable representing a predetermined binary value, and wherein each SRAM cell is an asymmetric SRAM cell having reduced leakage power with respect to a comparable symmetric SRAM cell, each asymmetric SRAM cell comprising:

a plurality of transistors operably coupled and configured as an asymmetric SRAM cell, wherein the plurality of transistors include at least one of a first type of transistor and at least one of a second type of transistor that is weaker than the first type of transistor, such that the configuration of each asymmetric SRAM cell achieves reduced leakage power with respect to a symmetric SRAM cell having the first type of transistor only; and

at least one sense amplifier comprised of:

a first pair of cross coupled inverters across a bitline (BL) and a bitline bar (BLB);

a second pair of cross coupled inverters operably coupled with the first pair of cross coupled inverters;

a plurality of additional sense amplifier transistors forming a dummy column of cells that store a second predetermined binary value at all times wherein during a read operation of the SRAM cell one of the dummy cells will have its wordline asserted, said dummy column of cells operably coupled with the first pair of cross coupled inverters; and

four inputs operably coupled with a subset of the sense amplifier transistors wherein the inputs include the BL, the BLB that derive from the SRAM cell, a dummy bit line (D), and a dummy bitline bar (DB) that are input to the dummy cells such that D is input to the sense amplifier on the same side as BLB while DB is input to the sense amplifier on the same side as BL.

10. (Original) The combination SRAM device and sense amplifier of claim 9 wherein the sense amplifier transistors coupled with BL and BLB have higher transconductance characteristics than the sense amplifier transistors coupled with D and DB.

11. (Original) The combination SRAM device and sense amplifier of claim 9 wherein at least one of the sense amplifier transistors coupled with BL and BLB are selected from among the group consisting of:

transistors having a lower voltage threshold (V_t) as compared to the voltage threshold (V_t) of the transistors coupled with D and DB;

transistors having a increased channel width as compared to the channel width of the transistors coupled with D and DB; and

transistors having a decreased channel length as compared to the channel length of the transistors coupled with D and DB.

12. (Original) The combination SRAM device and sense amplifier of claim 9 wherein the SRAM device comprises an SRAM device selected from the group consisting of a direct store SRAM device and a selectively inverted SRAM device.

13. (Original) The combination SRAM device and sense amplifier of claim 12 wherein the array of SRAM cells in the SRAM device comprises a cache memory selected from the group consisting of a direct store cache memory and a selectively inverted cache memory.

14. (NEW) An asymmetric static random access memory (SRAM) cell operable with a supply voltage to store a one or a zero, the asymmetric SRAM cell further comprising:

at least two cross-coupled inverters, one having an output electrically connected to a bit line bar when a word line is held high and the other having an output electrically connected to a bit line when a word line is held high and further comprising a pull-down transistor; and

a pass transistor connected to a gate of the pull-down transistor so that a voltage across the gate is reduced relative to the supply voltage, thereby reducing leakage through the gate when the asymmetric SRAM cell is storing a zero.

15. (NEW) The asymmetric SRAM cell of claim 14 wherein a voltage at a gate of the pass transistor is reduced relative to the supply voltage to further reduce leakage through the gate of the pull-down transistor.

16. (NEW) The asymmetric SRAM cell of claim 14 wherein the first and second inverters comprise a plurality of transistors further comprising at least one first type of transistor and at least one second type of transistor that is weaker than the first type of transistor.

17. (NEW) The asymmetric SRAM cell of claim 16 interconnected with a plurality of like SRAM cells and a sense amplifier further comprising pairs of cross-coupled inverters and a plurality of sense amplifier transistors forming a dummy column of cells.